MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

TRANSISTOR SHIFT REGISTERS

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ABSTRACT

Three different types of high-speed transistor shift registers are discussed. The high speed (3 to 5 microseconds per shift pulse) is made possible by the use of one- and two-transistor nonsaturating bistable circuits. The design of these circuits and their limitations when used as shift register stages is discussed.

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TRANSISTOR SHIFT REGISTERS

I. INTRODUCTION

In general, shift registers are composed of a chain of interconnected bistable elements. When desired, the device may be made to perform such operations as sampling, coding, decoding, storing, and so forth.

This paper describes three different types of nonsaturating* bistable circuits, two of which may be used as the bistable elements necessary to construct shift registers. The third circuit offers a convenient method of building a sampling device such as a matrix switch. The shift-register logic is essentially the same as that used with vacuum tubes, that is, between each bistable stage is a diode "and" gate which controls the state of the succeeding stage.

In Sec. II, we present two of the basic circuits and describe the static bistable characteristics of each. Section III shows the shift-register logic used. Section IV gives an analysis of the single- and double-transistor bistable circuits. Section V discusses the specialized transistor shift register, and in Sec. VI we discuss the limitations of each as to speed, reliability, etc.

II. THE BISTABLE CIRCUITS

A. The Negative-Resistance Bistable Circuit[1]

In order to avoid the problems arising in saturated transistor circuits, the circuit of Fig. 1 was devised.[1]

The diode D_1, and resistor R_e, along with V_{ee} and V'_{ee}, present the broken load line $R'_e R_e$ to the transistor emitter input characteristics. This is shown in Fig. 2. When the transistor is in the high conducting state (Point b, Fig. 2), the emitter voltage V_e is equal to V_{ef}. Point b is short-circuit unstable, therefore it is necessary that R_e be larger than the negative transistor input resistance $-R_N$. Moreover, the capacitance at the emitter must be kept small (see Sec. IV). The second point (a) occurs when the transistor is inactive. Hence we have a single-transistor bistable circuit with two nonsaturated stable states.

B. The Two-Transistor Nonsaturating Flip-Flop[2]

The circuit shown in Fig. 3(a) was devised to avoid the effects of minority-carrier storage[3] that arise in saturated flip-flops. In order to explain the circuit characteristics, we break the circuit in a symmetrical way as in Fig. 3(b) and plot the input characteristics in Fig. 3(c). Points a and b are the only stable points since the positive input resistance of the "off" transistor in parallel with R_e exceeds in magnitude the negative input resistance of the "on" transistor.[1] Point c, where both transistors are on, is unstable since both transistors have negative input resistances. The current I is kept smaller than I_{ev} to avoid operation in the saturated region.

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*A bistable circuit that has active points in the negative-resistance region.

III. THE TRANSISTOR SHIFT REGISTER

A. Single Transistor Per Stage

A shift register may be formed from the bistable element discussed in Sec. 2 by inserting diode gates between each stage. This is shown in the block diagram of Fig. 4. The first stage is "set" (switched from Point a to Point b, Fig. 2) by clock pulses that are controlled by the input binary code. When Stage 1 is set, the diode gate allows a clock pulse to set the second stage. Stage 2 "resets" Stage 1 and allows the next clock pulse to set the third stage, etc. In this manner, the "sense" of the first stage may be transferred down the chain of bistable elements.

For a detailed three-stage schematic of the shift register, see Fig. 5. In Fig. 6 is shown an analysis of the waveforms at various points of the circuit.

B. The Flip-Flop Shift Register

The flip-flop shift register is formed from the bistable elements in the same way as with vacuum-tube shift registers, that is, the inputs to a particular stage are the clock pulses that have been gated from the outputs of the previous stage; this is shown in Fig. 7.

IV. ANALYSIS AND DESIGN OF THE ONE- AND TWO-TRANSISTOR BISTABLE CIRCUITS

There are several factors that complicate the design of the transistor bistable circuits necessary to construct high-speed shift registers. First, the variations in transistor parameters from unit to unit necessitate that the basic design of the bistable circuit be stable over quite large percentage changes in operating points. Second, since most presently available transistors (Type BTL 1689) have relatively low-frequency cutoffs (less than 5 Mc), the trigger pulse must be controlled in both amplitude and width.[1,4] Third, since the input impedance of a point-contact transistor circuit is, in general, lower than the output impedance, cascading stages becomes difficult.

From Figs. 5 and 6, we see that the "reset" capacitor (Point h) must recover through the series combination of resistances R_2 and R_s. Thus, to increase the maximum operating speed, the triggering capacitors must be made as small as possible. To determine the minimum value capacitors that will suffice to reliably switch the nonsaturating bistable circuits, a transient analysis must be made.

We may dynamically represent the large-signal transistor equivalent circuit devised by Adler[5] as in Fig. 8.

When the static case is considered, the current in the constant-current generator becomes $\alpha_e i_e$. In the dynamic case, i_g is related to i_e as in Fig. 8. It is evident that i_g satisfies the equation

$$\tau \frac{di_g}{dt} + i_g = i_e \quad , \tag{1}$$

where $\tau = RC$.

Figure 8 and Eq. (1) indicate the fact that we are inserting the frequency dependence

of the transistor into the current i_g, and maintaining a frequency-independent α_e. This is completely equivalent to the assumption that the generator current is equal to $\alpha_e i_e$ where $\alpha_e = (\alpha_{e0})/(1 + \tau s)$.

The negative-resistance bistable circuit may then be dynamically represented as shown in Fig. 9. The differential equation for i_g when the transistor is in the active region is:

$$\frac{d^2 i_g}{dt^2} + \frac{di_g}{dt}\left(\frac{R_e + R_p}{C_e R_e R_p} - \frac{R_N}{R_p \tau}\right) - i_g\left(\frac{R_N - R_e}{R_e R_p C_e \tau}\right) + \frac{V_{ee} - V_p}{R_p R_e C_e \tau} \quad , \tag{2}$$

where

$$R_N = \frac{R_b[(\alpha_e - 1) r_c - R_L]}{R_{ct}} \quad , \qquad R_{ct} = R_L + r_c + R_b \quad ,$$

$$R_p = R_b \frac{r_c + R_L}{R_{ct}} \quad , \qquad V_p = V_{cc} \frac{R_b}{R_{ct}} \quad ,$$

and C_e is the effective capacitance between emitter and ground.

R_N is the magnitude of the slope of the negative-resistance portion of the emitter input characteristics (Fig. 2). R_p is the negative of R_N with $\alpha_e = 0$. V_p is the magnitude of the peak-point voltage.

The solution of Eq. (2) is the sum of two exponentials, the frequencies of which are given by:

$$\omega^2 + \omega\left(\frac{R_e + R_p}{C_e R_p R_e} - \frac{R_N}{R_p \tau}\right) + \frac{R_e - R_N}{R_e R_p C_e \tau} = 0 \quad . \tag{3}$$

Since the third term of Eq. (3) is positive ($R_e > R_N$), the ω's will both have the same algebraic sign. If the second term is negative, both ω's will be positive. Under this condition, the "on" point will be unstable. Therefore, the condition for stability is:

$$\tau > \left(\frac{R_N}{R_p}\right)\left(\frac{R_e R_p C_e}{R_e + R_p}\right) \approx R_N C_e \quad , \tag{4}$$

or, in terms of frequency cutoff,

$$f_{c0} < \frac{1}{2\pi R_N C_e} \quad . \tag{5}$$

A. Triggering Requirements of the Negative-Resistance Bistable Circuit

Turn ON

Consider the circuit shown in Fig. 10. In order to be sure that the negative-resistance bistable circuit will switch (change states) reliably, it is necessary that the trigger pulse exceed a given amplitude for a given period of time.[1,4] Moreover, the amplitude-width requirement is different depending upon the state of the circuit[1,4] and the frequency response of the transistor. Consider only the "set" (turn on) function of the circuit shown in Fig. 10. The circuit may be redrawn, inserting the dynamic transistor equivalent circuit, to that of Fig. 11.

Solving the loop equations, the following expression may be obtained for i_g:

$$\frac{d^2 i_g}{dt^2} + \frac{di_g}{dt}\left(\frac{1}{\tau} + \frac{R_p + R_e}{C_1 R_e R_p}\right) + i_g\left(\frac{R_e - R_N}{C_1 R_e R_p \tau}\right) - \frac{V_{cc} + V_p}{C_1 R_e R_p \tau} \quad . \tag{6}$$

The solution of Eq. (6) is the sum of two exponentials, the frequencies of which are given by

$$\omega^2 + \omega\left(\frac{1}{\tau} + \frac{R_e + R_p}{C_1 R_e R_p}\right) + \frac{R_e - R_N}{C_1 R_e R_p \tau} = 0 \quad , \tag{7}$$

or

$$i_g = A_1 \exp[\omega_1 t] + B_1 \exp[\omega_2 t] + I_f \quad , \tag{8}$$

where

$$I_f = \frac{V_{ee} + V_p}{R_e - R_N} \quad .$$

I_f is the steady-state value of i_e when the circuit is in the "on" state. Solving the loop-current expression for i_e yields

$$i_e = A_1(1 + \tau\omega_1) \exp[\omega_1 t] + B_1(1 + \tau\omega_2) \exp[\omega_2 t] + I_f \quad . \tag{9}$$

From the initial conditions,

$$A_1 = \left(\frac{1}{\omega_1 - \omega_2}\right)\left(\frac{I_0}{\tau} + I_f\omega_2\right) \quad , \tag{10a}$$

$$B_1 = \left(\frac{1}{\omega_2 - \omega_1}\right)\left(\frac{I_0}{\tau} + I_f\omega_1\right) \quad , \tag{10b}$$

where $I_0 = (V_t + V_{ee})/(R_e)$, and is defined as the value of i_e just after the trigger pulse is applied.

Since R_e is greater than R_N, the third term in Eq. (7) is positive, hence ω_1 and ω_2 are negative. The initial shape of i_e then, is a positive step, the amplitude of which depends upon V_t, followed by a converging decay. Since i_g tries to follow i_e, the eventual circuit state is dependent upon the relative magnitudes of i_e and i_g as time progresses. For when i_e decays to I_x (Fig. 2), diode D_1 closes and R_e becomes R_e'. Since R_e' is less than R_N, the third term in Eq. (7) is negative and the circuit is unstable. In order for the circuit still to switch on, even though i_e becomes less than the value I_x, the rate of change of i_e must, at some time after t_x, be equal to zero (t_x is defined as the time at which i_e is equal to the value I_x); that is

$$\left.\frac{di_e}{dt}\right|_{t = t_\Delta} = 0 \quad , \tag{11}$$

where

$$t_x < t_\Delta < \infty \quad , \tag{12}$$

and

$$i_e \Big|_{t = t_x} = I_x \quad , \tag{13}$$

At the time t_Δ, i_t is equal to zero; hence the circuit of Fig. 11 becomes that of Fig. 12.

The approximate triggering criterion for the circuit of Fig. 12 is

$$i_g(t_x) > I_N \qquad \text{Turn on} \quad , \tag{14a}^{1,4}$$

$$i_g(t_x) < I_N \qquad \text{Turn back off} \quad . \tag{14}$$

The values of C_1 as a function of the trigger voltage V_t that will fulfill the condition Eq. (14a) appear in Fig. 13. The results are found to be in good agreement with experimental data.

Turn OFF

The approach that may be used to determine the "turn off" trigger requirement is the same as for the turn-on case; using the appropriate equivalent circuit, we solve the pertinent loop equations, define the turn off criterion, and solve for the minimum trigger voltage that will suffice to switch the circuit.

Since the circuit is turned off by applying a positive pulse to the base, the transistor emitter is instantaneously switched off (Fig. 10). Therefore, the turn-off analysis may be based upon the circuit shown in Fig. 14.

Figure 15 indicates the action of the circuit shown in Fig. 14. At time t_0, i_e starts increasing. The same arguments as in the previous section show that, in order for the circuit to switch off, i_e must go to zero. As in the case of turning on, the triggering diode D_3 will open when the rate of change of i_e is equal to zero. Hence

$$i_g(t_\Delta) > I_N \qquad \text{Turn back on} \quad , \tag{15a}^{1,4}$$

$$i_g(t_\Delta) < I_N \qquad \text{Turn off} \quad , \tag{15b}^{1,4}$$

where

$$t_0 < t_\Delta < \infty \quad , \tag{16}$$

$$i_e \Big|_{t = t_0} = 0 \quad . \tag{17}$$

If we denote by t_N the time required for i_g to decay from I_f to I_N, the approximate turn-off criterion may be stated as

$$t_0 > t_N \quad , \tag{18}$$

where

$$t_N = \tau \ln \frac{I_f}{I_N} \quad .$$

Figure 16 shows a comparison between the theoretical and experimental data when V_t is plotted as a function of C_2.

B. The Two-Transistor Nonsaturating Flip-Flop[3]

We may replace the transistors in the circuit of Fig. 3(a) by the equivalent circuit shown in Fig. 8. When this is done, the circuit of Fig. 17 is obtained, where the battery V_t implies that we are triggering on transistor B by applying a negative pulse to the base. The circuit of Fig. 17 may be analyzed by the same techniques described above. The solutions for the various current equations will be of the same form, although slightly more complex due to the circuit configuration. As above, the triggering requirements have a definite minimum amplitude-width relationship. This analysis is made elsewhere,[6] therefore it will not be repeated. However, an important point should be noted: the two-transistor flip-flop will trigger on narrower pulses than will the negative-resistance bistable circuit. This is because, although we are triggering at the base of transistor A (Fig. 17), and hence the same conditions apply as when triggering the single transistor, transistor B is being triggered at the emitter. Since the circuit is short-circuit unstable at the emitter, the currents in transistor B decay (or increase, as the case may be) with positive exponentials. This causes faster switching of transistor B, which in turn will cause the circuit to switch faster.

V. A SPECIALIZED TRANSISTOR SHIFT REGISTER[7]

A logical extension of the circuit shown in Fig. 3(a) is the multistage circuit of Fig. 18 where several transistor stages have their emitters tied to a common load resistor. As in the two-transistor case, only one transistor can conduct at a time, since any state with more than one transistor in the negative-resistance region is unstable.

A specialized shift register may be based upon this idea, as shown in Fig. 19. Suppose a negative pulse is applied to the base of the first stage. This stage will then be conducting and the others nonconducting. The sense of this first stage may then be propagated down the register by clock pulses gated to the stages sequentially.

The number of stages that may be connected together is limited by two factors. First, the total accumulated capacitance between emitter and ground must be kept small enough to render each transistor stable [Eq. (5)]. Second, the resistance between emitter and ground, which is reduced by the addition of more transistors, must be kept large enough to render each transistor's on operating point in the negative-resistance region.

As many as ten transistors may be connected in this manner with little or no difficulty. We may construct a long register, using this method, as shown in Fig. 20.

VI. COMPARISON AND EVALUATION

An over-all analysis of the shift-register circuits reveals the following facts: first, a point-contact transistor switching circuit requires a definite, predictable, minimum pulse-height width relationship that is a function of the transistor frequency response and the circuit configuration; secondly, the maximum speed of operation of a system constructed from these circuits is limited, not by the switching time of the circuits, but by the recovery time of the

associated triggering capacitors. In view of this, when designing high-speed systems, it is advantageous to use circuits with (a) high input impedance, and (b) as low recovery resistance as possible for the triggering capacitor circuits.

The above results appear to exclude the possibility of using saturated bistable circuits with a high degree of reliability due to the turn off triggering time.[1]

Exhaustive tests have been made on each of the shift registers described above. The two-transistor flip-flop works reliably with 80 per cent of all BTL 1698 transistors at rates up to 5 μsec per shift pulse. The shift register constructed from the negative-resistance bistable circuit will operate up to 6 μsec per stage. However, at these fast rates, the coupling capacitors must necessarily be small, and this shift register therefore is less reliable than the flip-flop shift register. At lower rates, the coupling capacitor may be larger with correspondingly greater reliability. The specialized shift registers offer a good reliability up to 3 μsec per shift pulse when a maximum of 9 stages is connected to the common bias resistor, R_e. Longer registers should be connected as shown in Fig. 20.

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2. A. W. Carlson, "A Transistor Flip-Flop with Two Stable Nonsaturating States," AFCRC Report, December 1952.
3. R. A. Bradbury, "Hole Storage or Turn Off Time," AFCRC December 1952.
4. R. H. Baker, "Transistor Shift Register," M.S. Thesis, M.I.T., June 1953 (E. E. Dept).
5. R. B. Adler, "A Large Signal Equivalent Circuit for Transistor Static Characteristics," M.I.T., R. L. E. Transistor Group Report T-2, August 1951.
6. R. E. McMahon, I. L. Lebow, R. H. Baker, "A Two Transistor Shift Register," Lincoln Laboratory, M.I.T., M24-20, May 1953.

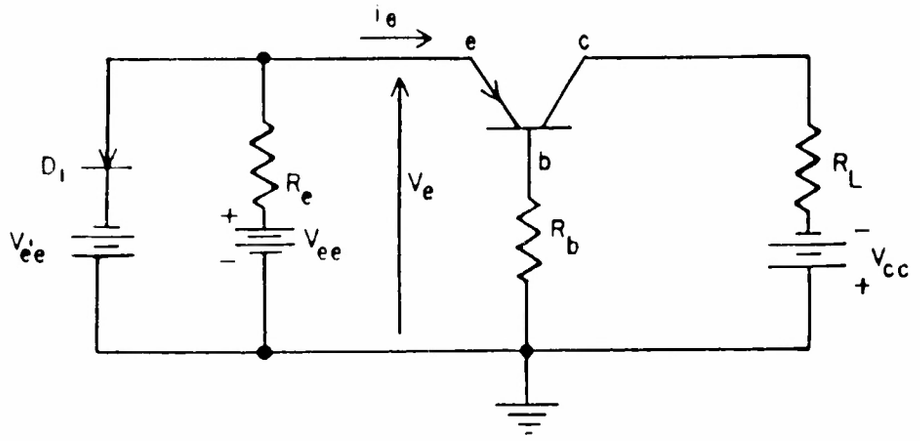


Fig. 1. Negative-resistance bistable circuit.

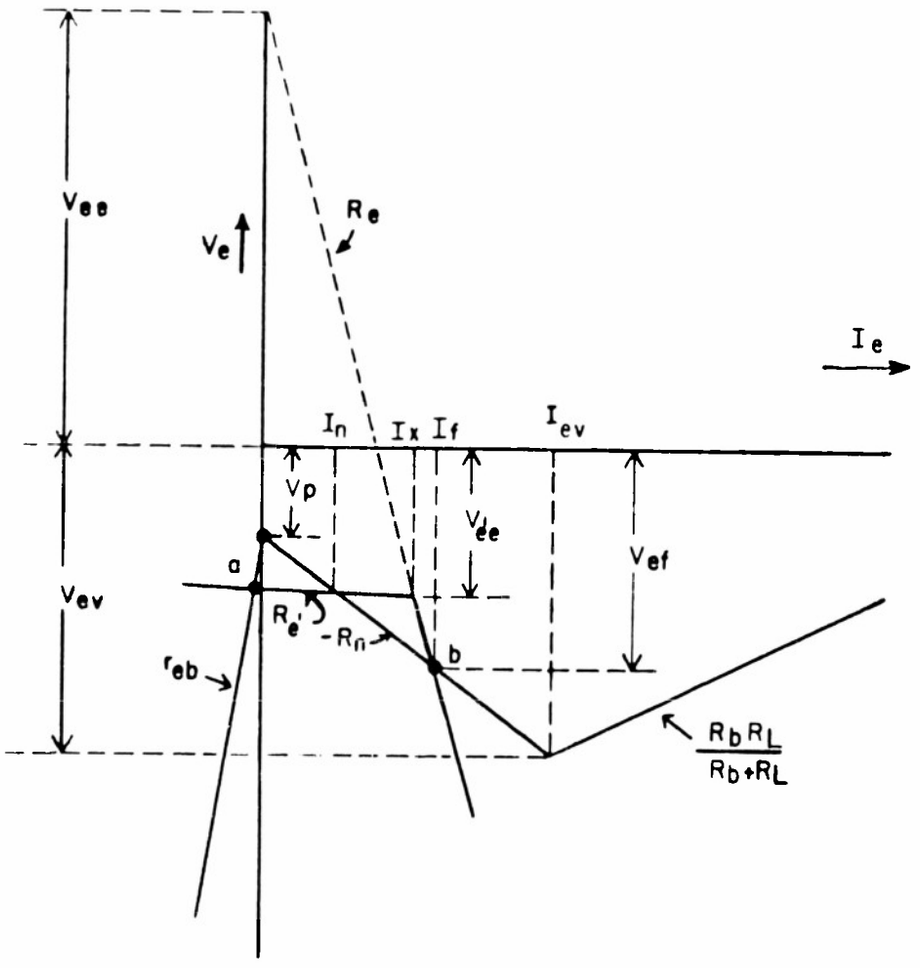


Fig. 2. Static emitter voltage-current characteristics.

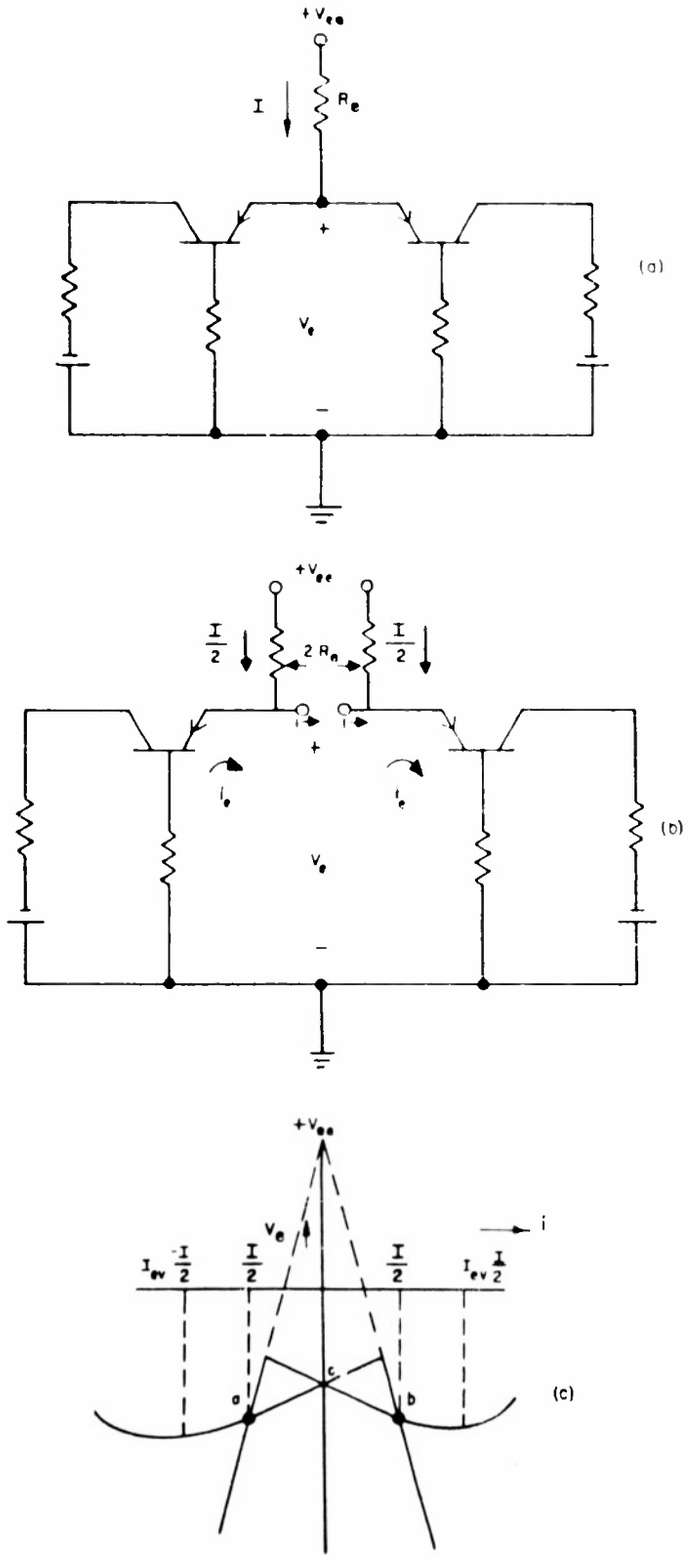


Fig. 3. Nonsaturating flip-flop.

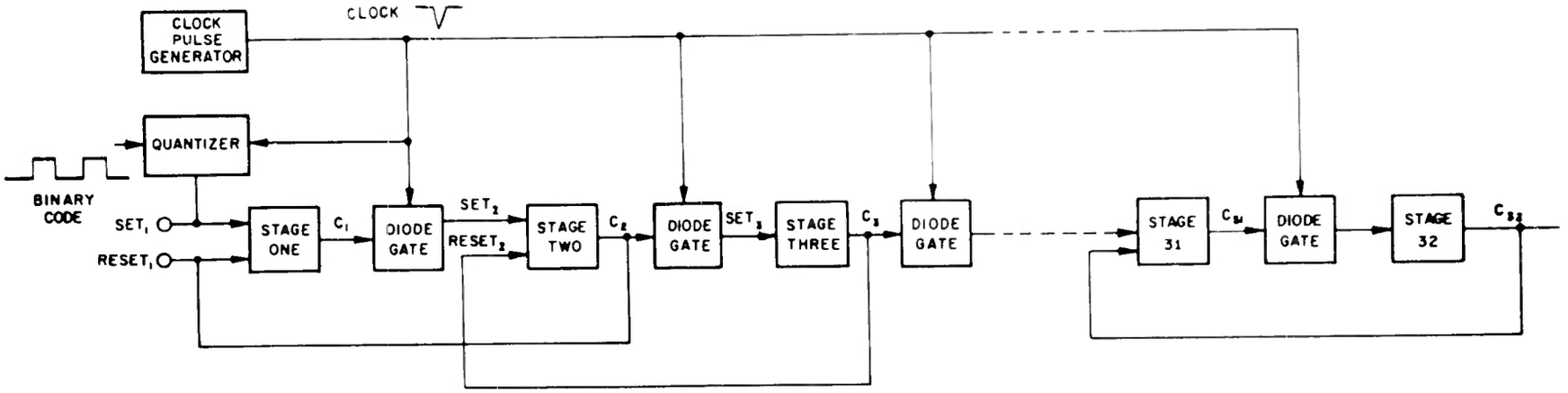
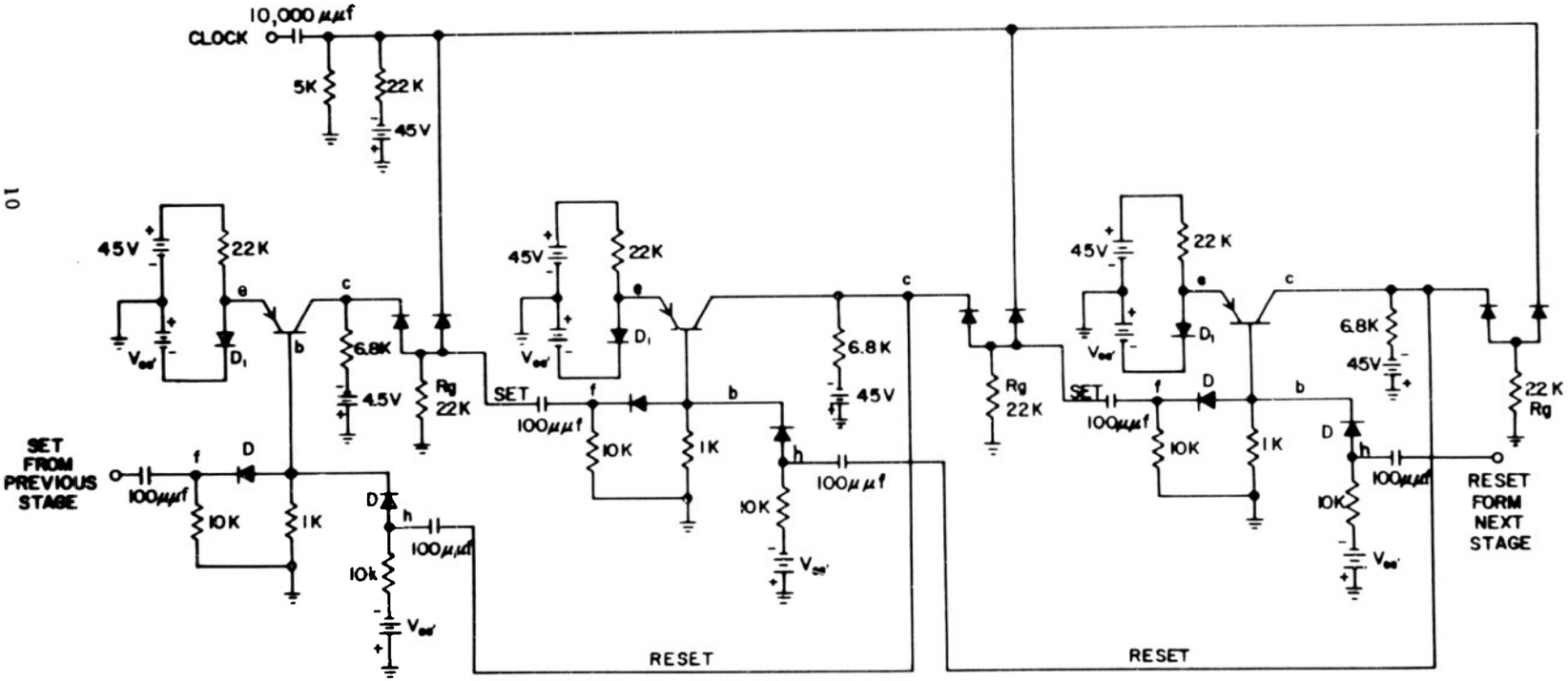


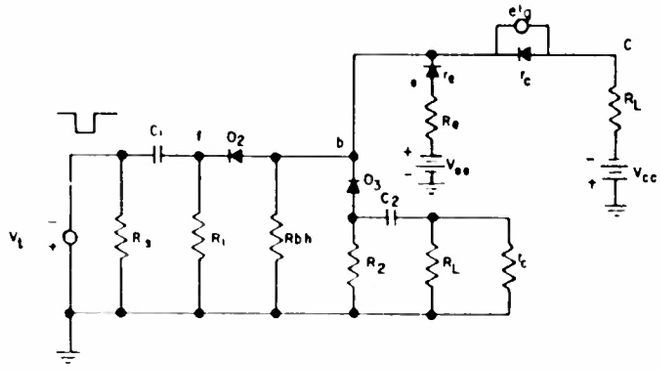
Fig. 4. Block diagram of single-transistor-per-stage shift register.



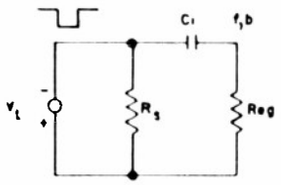
ALL DIODES ARE SYLVANIA TYPE IN 34A
ALL RESISTORS ARE $\frac{1}{8}$ WATT
$V_{cc'}$ = 3 VOLTS

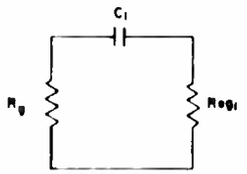
DRAWN FOR E. M. BAKER
DRAWN BY GERALDINE B. BARRETT
APRIL 29, 1963
C-KK-5

Fig. 5. Circuit diagram of single-transistor-per-stage shift register.



R_s (CLOCK SOURCE RESISTANCE) ≈ 0





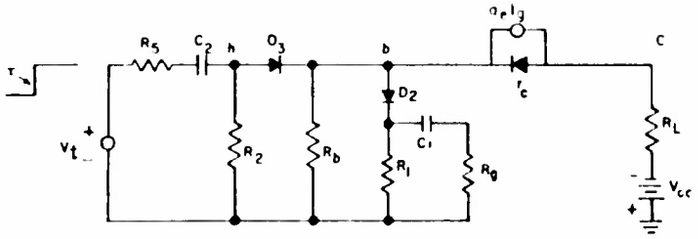
AFTER PULSE IS REMOVED

$R_s \approx 0$

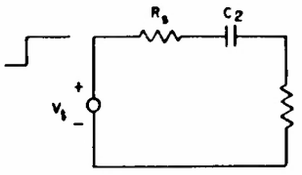
$R_{eg} \approx R_b \| R_1 \| R_2 \| R_L \| r_c \| (r_c + R_2)$

WHILE PULSE IS PRESENT

TRIGGER ON EQUIVALENT CIRCUITS

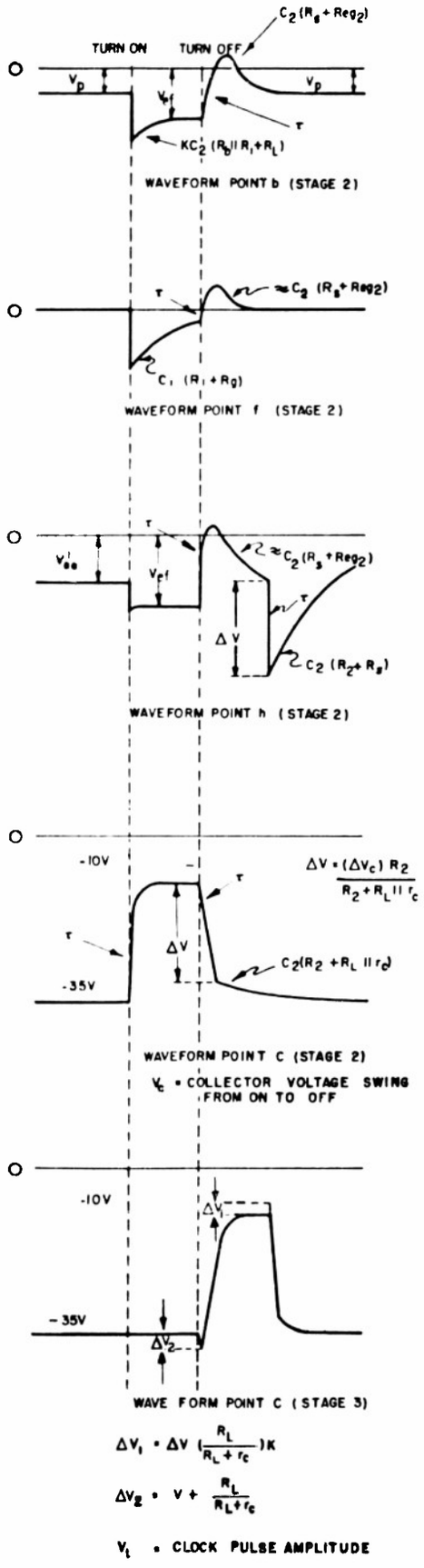


$R_s \approx R_L \| r_c$



$R_{eg_2} \approx R_2 \| R_b \| R_1 \| R_g \| (r_c + R_L)$

TRIGGER OFF EQUIVALENT CIRCUITS



$\Delta V_1 = \Delta V \left(\frac{R_L}{R_L + r_c}\right) K$

$\Delta V_2 = V + \frac{R_L}{R_L + r_c}$

V_t = CLOCK PULSE AMPLITUDE

Fig. 6. Waveform analysis of single-transistor-per-stage shift register.

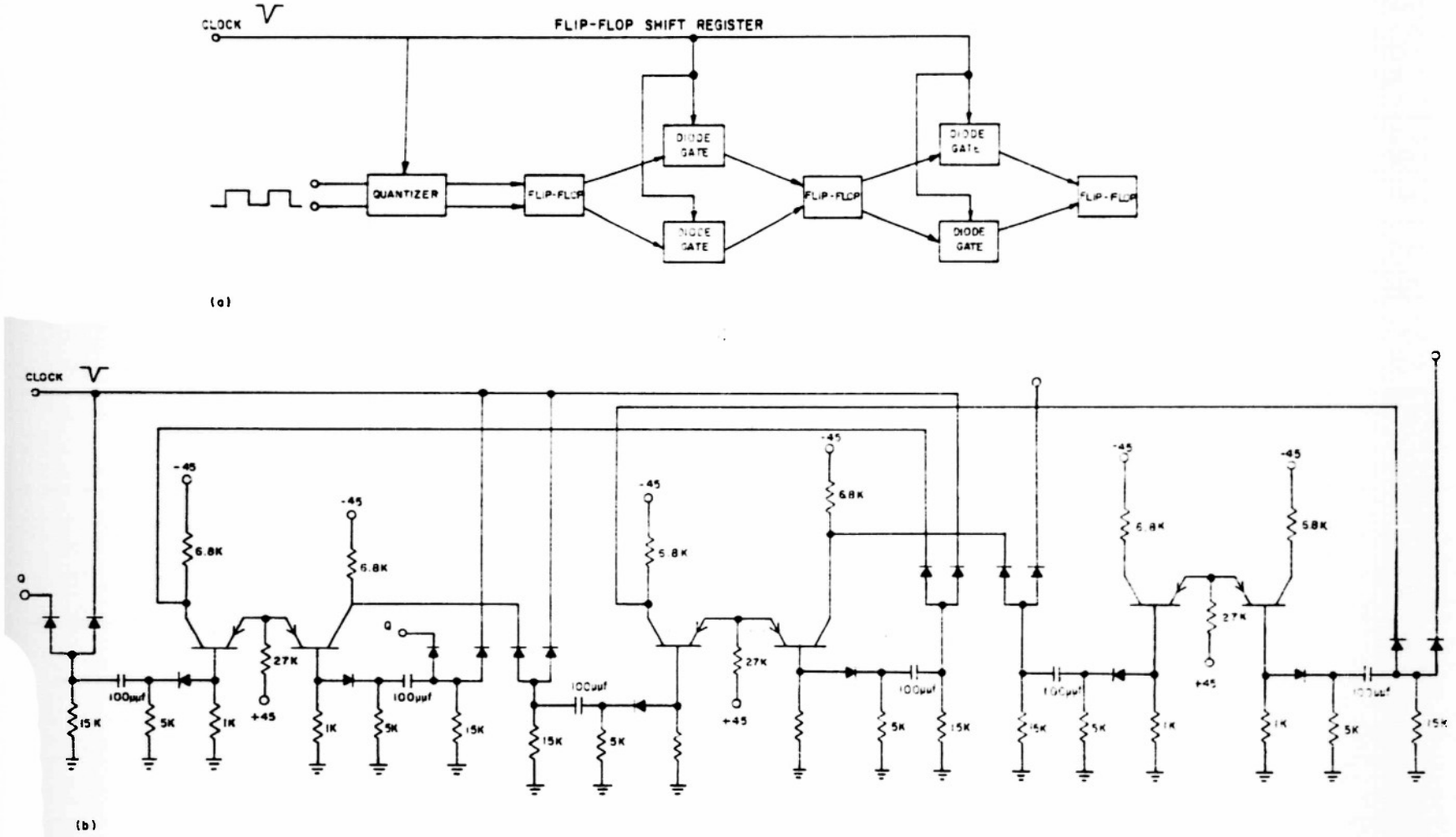


Fig. 7. Flip-flop shift register. (a) Block diagram; (b) circuit diagram.

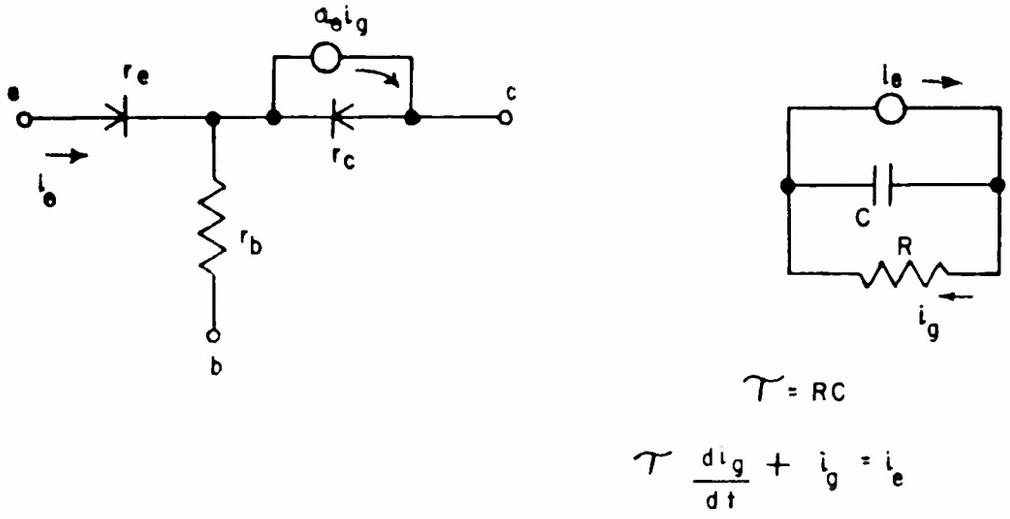


Fig. 8. Large-signal equivalent circuit for transistor dynamic characteristics.

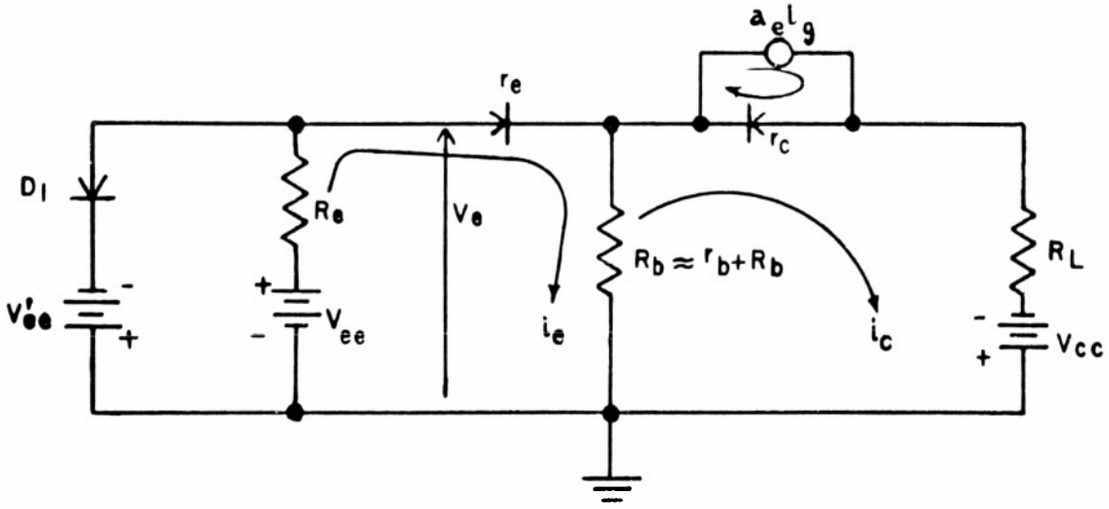


Fig. 9. Negative-resistance bistable circuit with transistor large-signal dynamic equivalent circuit.

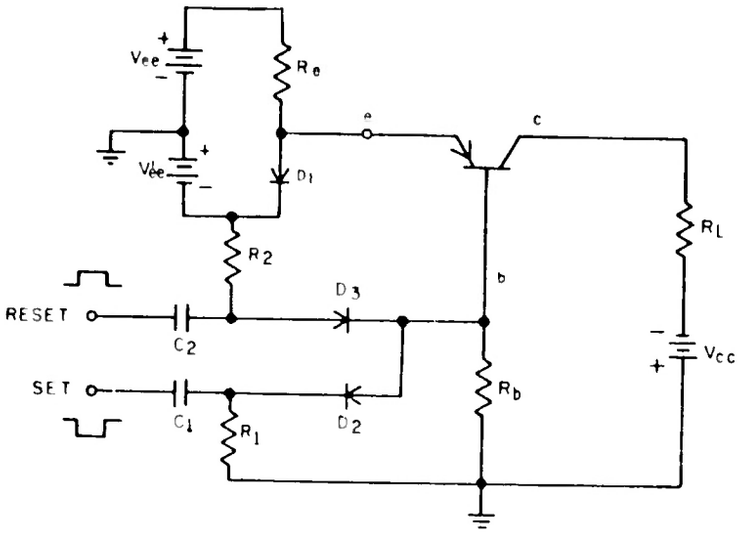


Fig. 10. Negative-resistance bistable circuit.

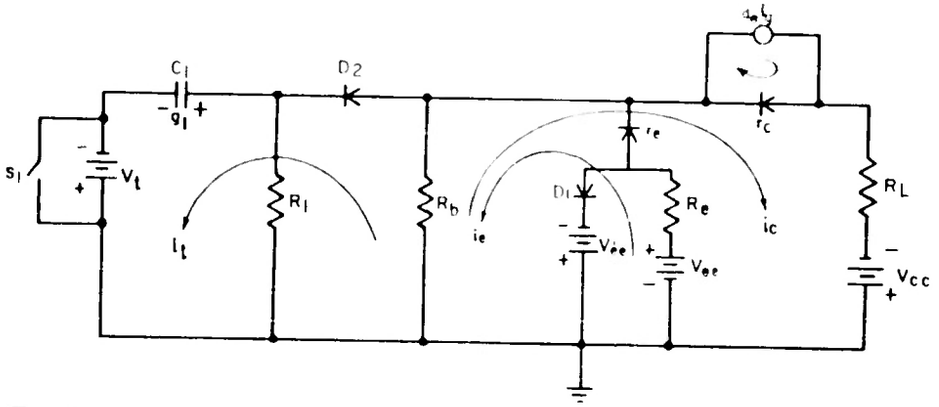


Fig. 11. Dynamic equivalent circuit for triggering on negative-resistance bistable circuit.

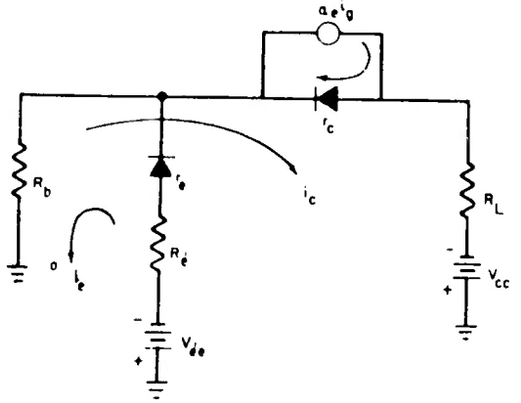


Fig. 12. Circuit of Fig. 11 after D_2 has opened.

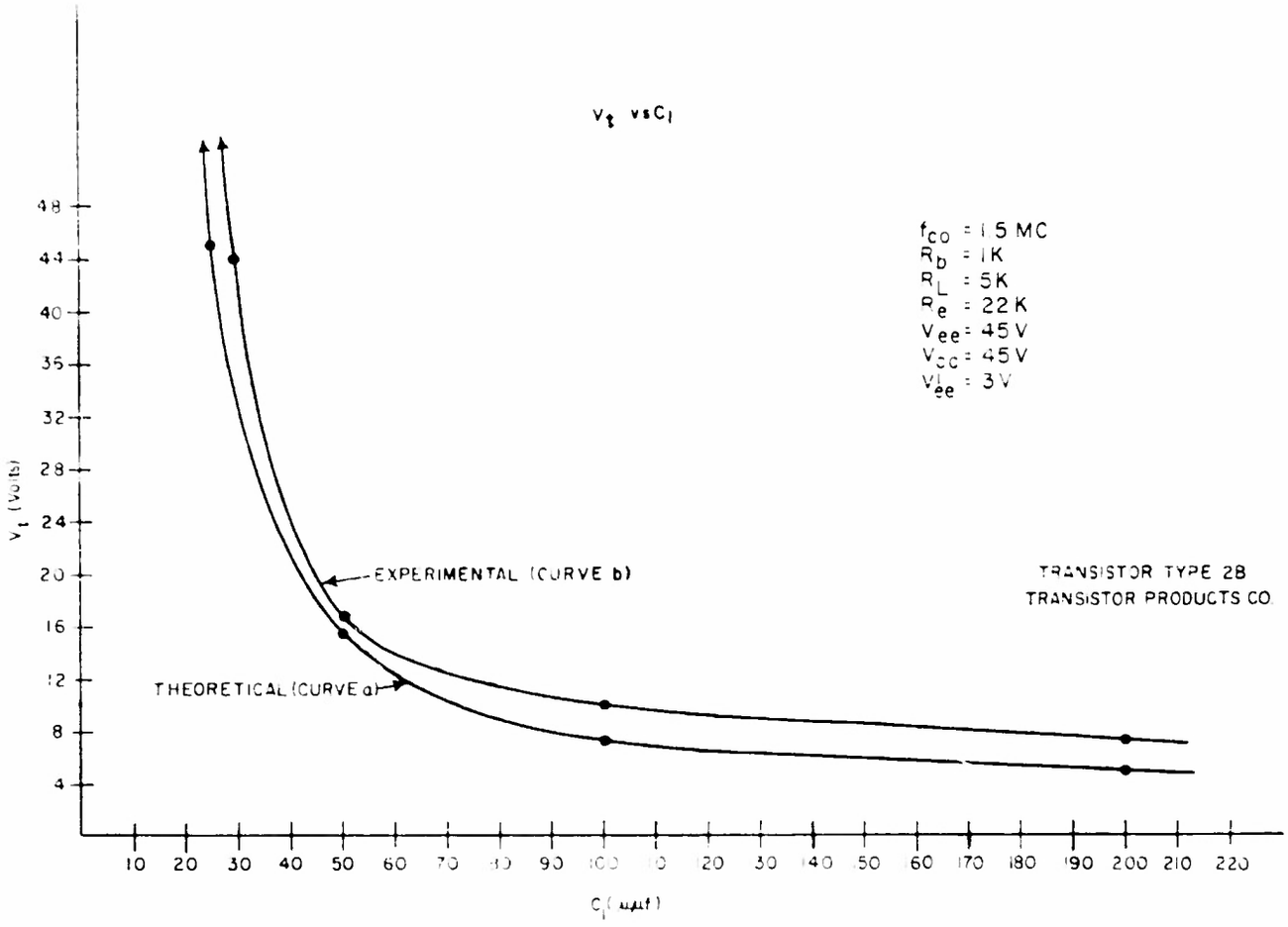


Fig. 13. Turn-on characteristic of negative-resistance bistable circuit.

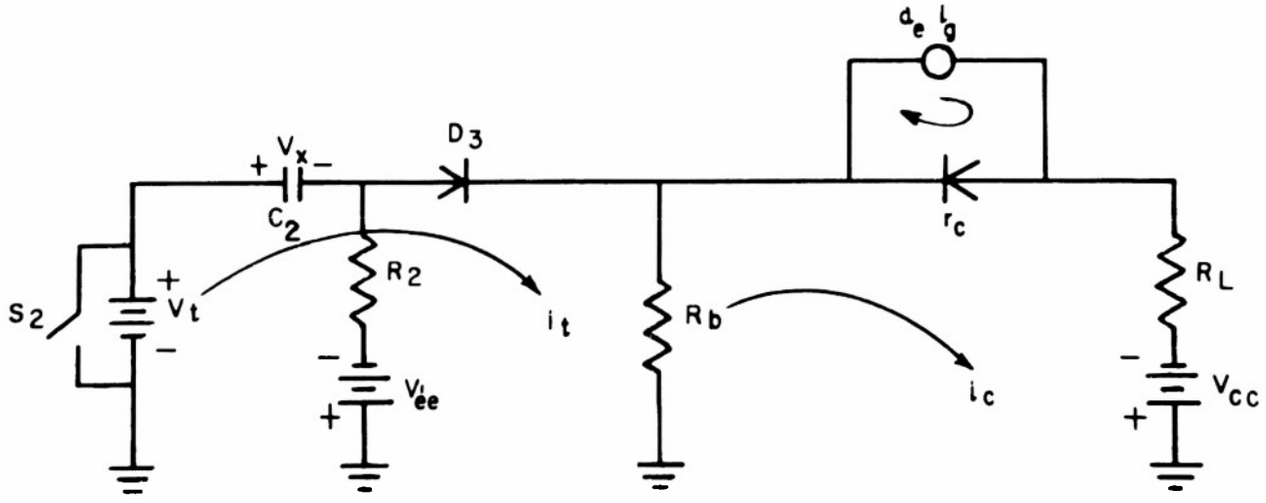


Fig. 14. Dynamic equivalent circuit for triggering off negative-resistance bistable circuit.

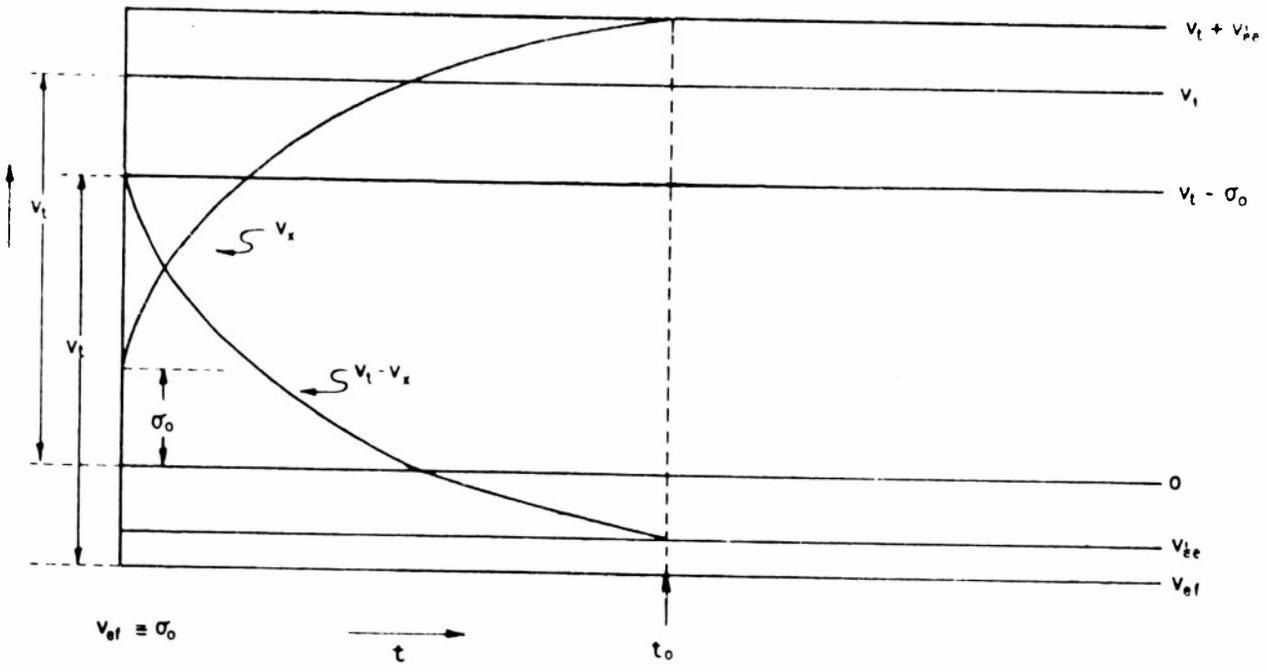


Fig. 15. Voltage waveforms for circuit of Fig. 14.

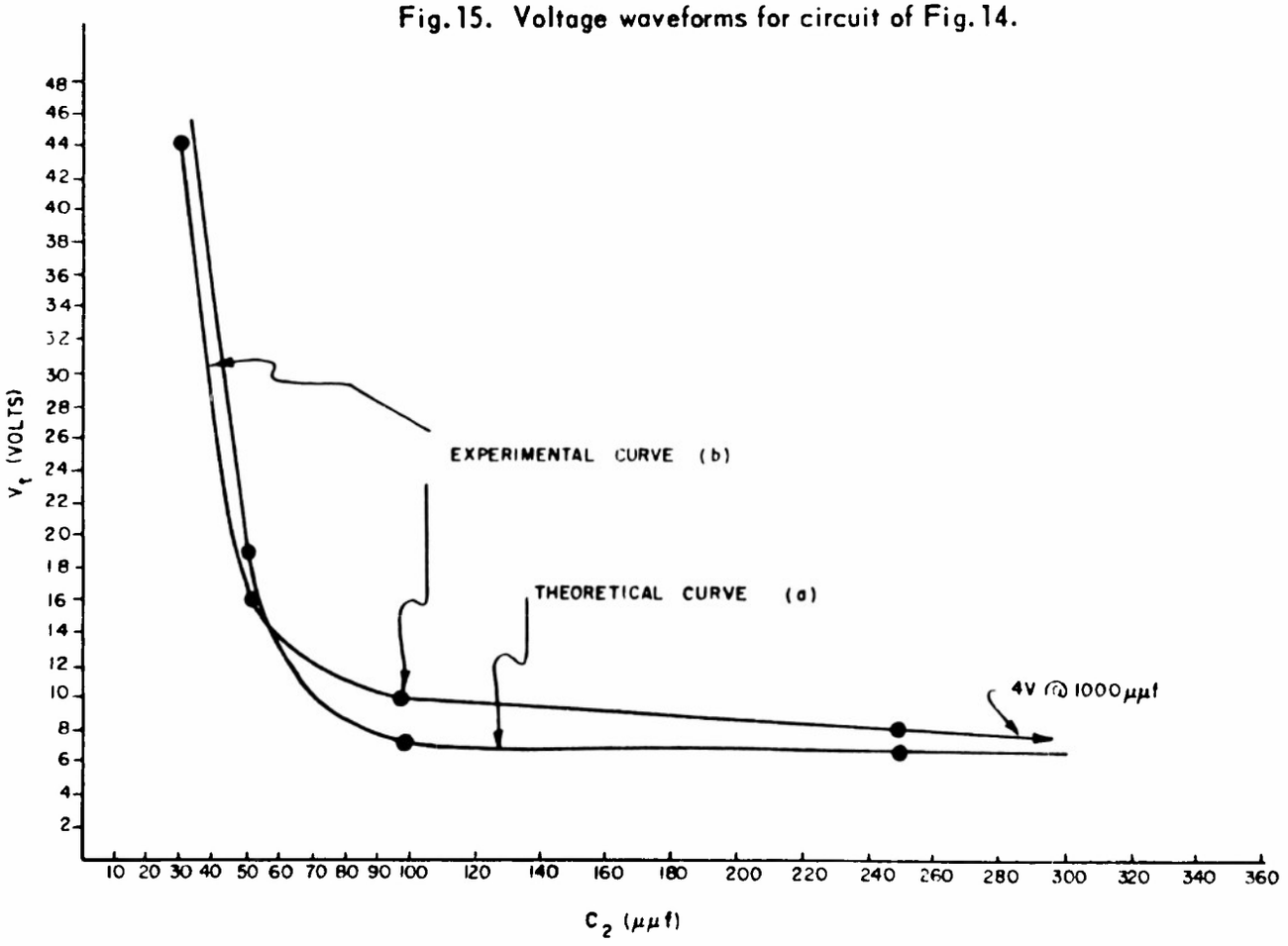


Fig. 16. Turn-off characteristics of negative-resistance bistable circuit.